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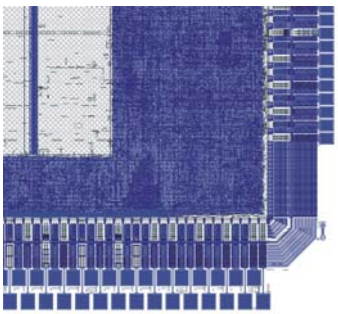
X-Stream T4 Chip Technical Overview



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Section 1 Summary

1.1 X-Stream T4 Highlights

- Four independently configurable media stream channels.
- eDOCSIS, DAVIC, and Starvue modems.
- Compliance with current and emerging standards, such as OCAP, DOCSIS, DOCSIS Set-Top Gateway (DSG), and Multi-Stream CableCARD™.
- Conditional access interface.
- XTend mini-cmts.
- Stream transcode processor.
- 656 digital video output port.
- Sub-system control and PCI host interface.
- Serial flash controller.
- Serial control ports.

1.2 X-Stream T4 Block Diagram

The figure below shows basic functions of the X-Stream T4.

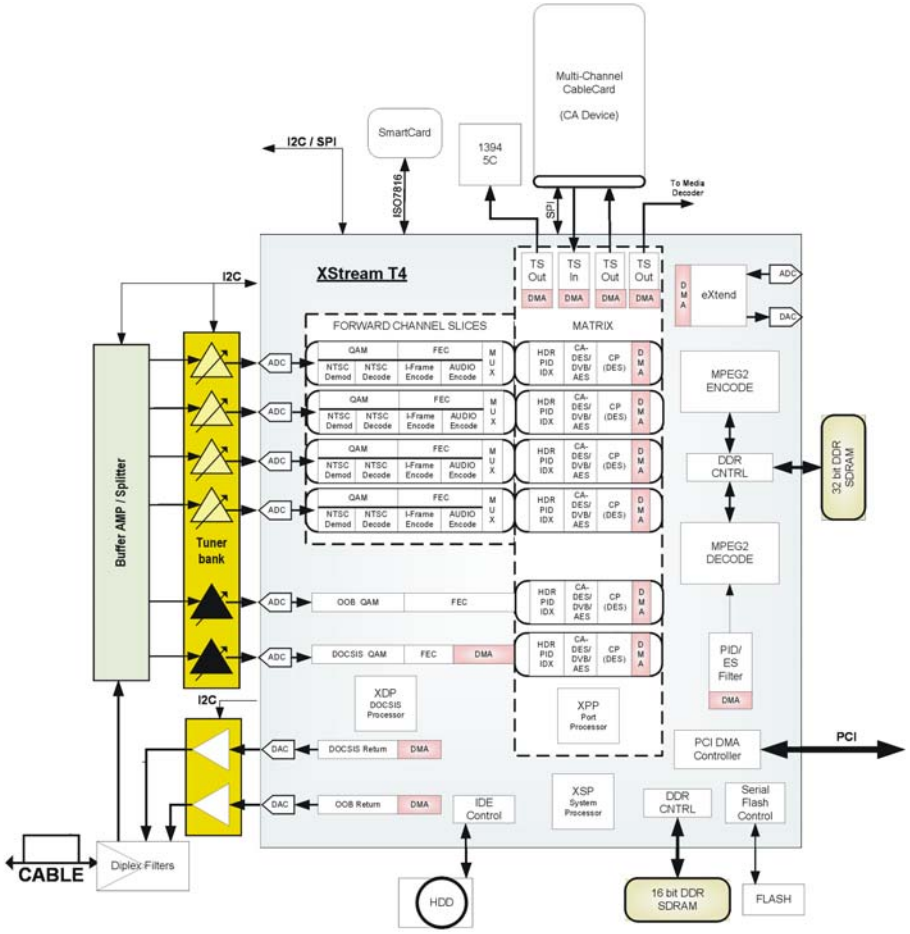

Figure 1-1: X-Stream T4 Block Diagram

Section 2 Features

2.1 Video Slices

The Digeo X-Stream T4 chip has four video channel slices. Each slice can be independently configured as either (1) a J.83b 64/256 QAM demodulator for digital channels or (2) an NTSC video demodulator for analog channels. When configured for NTSC, the demodulated video is MPEG-2 encoded using high quality I-Frame compression; the audio is encoded using MPEG-1 Layer 2 audio compression. The analog front end for a video slice is an integrated 10-bit ADC sampling at 44.75 MHz IF.

2.2 DOCSIS Cable Modem

- DOCSIS 1.1/2.0 based design.
- Upstream modulator supports TDMA, ATDMA, and S-CDMA.
- Hardware support for encryption, fragmentation, and concatenation.
- Downstream hardware support for three independent MAC/MAP/PDU DMA channels, SYNC processing, and packet header suppression.
- Independent servo tracking of CM timebase, modulation rate, and carrier.
- Enables Embedded DOCSIS Devices such as Set-Top Boxes, Portal Services to home data networks, and VoIP.

2.3 Out-of-Band (OOB) Support

The OOB support covers the downstream and upstream SCTE DVS 167 and SCTS DVS 178 requirements.

2.4 DDR SDRAM Controller

The X-Stream T4 contains a high-performance DRAM controller that provides an interface to a single, 16-bit wide DDR SDRAM chip with a capacity of 128 Mb, 256 Mb, or 512 Mb. The clock frequency matches that of the T4's internal processors.

Because the DRAM is a double data rate device, the internal interface is twice as wide as the external interface, while the external data transfer frequency is twice that of the internal interface. For a 166 MHz internal clock frequency, a DDR333 device would be used; it would provide a maximum bandwidth of 666 MBps. For a 200 MHz clock frequency, a DDR400 device would be used; the resulting maximum bandwidth would be 800 MBps. Note that the controller's efficiency is somewhat less than 100 percent. Consequently, the

actual bandwidth provided is significantly lower than the maximum values cited here.

2.5 Extend Video Distribution

The X-Stream T4 acts as a server. It supports multiple VP based thin clients in the home by including multiple QAM modulators (up to four) for audio, video and data distribution. Return path communication (from client to server) is based on a TDMA access scheme and handled by the T4 burst demodulator. The demodulators provide an IF interface to a cable driver.

Each QAM modulator provides a variable bandwidth (up to 12 MHz). The maximum bandwidth occupied by the 4 QAM is nominally 25.6 MHz. Modulation types are QAM64 and QAM256 compatible with ITU J83B specification for low-delay mode. The maximum usable bit rate achievable is 152 Mb/s.

On the return path, QPSK and QAM16 burst with known preambles are used. The TDMA access scheme synchronization is performed based on timing information embedded in the Downstream signal. The maximum data rate on the return path is 10.24 Mb/s shared between all slaves.

2.6 Digital A/V Ports

The X-Stream T4 provides a single digital audio/video port. The A/V port consists of an ITU-656 digital video port and an I2S digital audio port.

The digital video ports allow a fully demodulated NTSC video stream to be transferred out of the chip to external video compression or presentation hardware.

The decoded audio from NTSC channels can be output through the I2S ports for external MPEG audio encoding.

2.7 Internal Processors

The X-Stream T4 contains three internal processors: the X-Stream System Processor (XSP), the X-Stream DOCSIS Processor (XDP), and the X-Stream PID Processor (XPP). The internal bus architecture allows full access such that any processor can be used to access any module within the chip. The XSP controls the boot process.

- Secure Boot - A small, internal boot ROM is used to begin the boot process and to provide enhanced security capabilities. An external non-volatile device may also be employed to provide a unique serial number for additional security. The XSP verifies system identity and integrity before completing the boot process and allowing software operation.
- Conditional Access Algorithm Support - <TBD>

2.8 PCI 2.2 Compliant Interface

Target Features

- Fully PCI 2.2 compliant bus with support for 32-bit addresses.
- Medium decode of target transactions.
- Support for Single Access Cycles (SAC) for internal registers.

Initiator Features

- Fully PCI 2.2 compliant with support for 32-bit addresses and data.
- Capable of generating Memory Write and Invalidate, Memory Read Line, and Memory Read Multiple commands based on cache line size. If the cache line size is valid, Memory Read Multiple commands are issued for transfers greater than a cache line in size, and Memory Read Line commands are issued for transfers greater than two quad-words (but less than or equal to a full cache line).
- Support of cache line sizes of 8, 16, 32, 64, and 128 dwords.

PCI DMA Features

The primary PCI interface port has additional features that allow it to perform host PCI configuration functions for embedded PCI applications.

- Multi-threaded DMA Engine - Local Memory DMA engines from the BIC-3000 design are provided. This highly flexible DMA engine allows up to 256 DMA contexts to be active at any time. Automated EBUS low latency transfers are supported by the DMA engine.
- Chip Configuration - The PCI configuration space registers for the primary PCI port can be loaded during boot from the internal P1/0. This feature allows the device configuration data to be updated without the added cost of a dedicated EEPROM device.
- Special Cycles - The X-Stream T4 can monitor the PCI bus for Special Cycle commands. By default, this feature is disabled. The local CPU can enable the ability in the SBF (South Bridge Functions) Features Register. If Special Cycle monitoring is enabled and a Special Cycle is encountered, the contents of the SPC_RESET register are used to determine if the X-Stream T4 should issue a RESET on the PCI bus.

2.9 ATA-66 Disk Drive Interface

The X-Stream T4 contains two ATA/66 compatible host disk controllers, and each supports up to two drives in a master/slave configuration. The controllers support low speed, full speed, and high speed modes.

ATA Operation Modes

- Support for PIO timing modes 0, 2, 3, and 4.
- Support for Ultra DMA 0, 1, 2 (33), 3, and 4 (66).

Access to the IR ports from the PCI interface is available through the mailbox registers using the defined API.

2.10 MPEG-2 Transcoding

The X-Stream T4 includes an IBP MPEG-2 Encoder which allows the transcoding of I-Frame video from the video slices to lower bit rate IBP MPEG-2.

2.11 Transport Stream Processing

The X-Stream T4 contains six configurable transport processing engines (TEs) supporting the four video slices, OOB/DOCSIS, conditional access, and three independent transport stream out interfaces. The chip's stream processing block also includes some hardware assist for section filtering/verification and a serial interface for CableCard communication.

Each TE supports the following features:

- Filtering of up to 64 PIDs.
- Up to 16 different simultaneous DMA destinations.
- DES, Triple-DES, DVB or AES CA descrambling.
  - Up to 16 different Triple-DES and AES key sets.
  - Up to 48 different DSE and DVB key sets.
- DES, Triple-DES copy protection.
  - Up to two different Triple-DES key sets.
  - Up to six different DES key sets.
- MPEG PES start code indexing.
  - Up to 64 transport streams.
  - All or any subset of start codes may be captured for PIDs containing video data.
- Transport input.
  - Configurable for serial or parallel operation.
  - Support for Advanced Multistream CableCard.

Three transport out interfaces include:

- Serial or parallel output.
- Support for Advanced Multistream CableCard.

- Data direct from transport engine(s) or internal memory with or without PCR queuing.

The section processing logic supports the following:

- Section filter.
  - 64 total filters shared between all transport processing blocks.
  - Each filter is eight bytes.
  - Can be sub-divided into two independent groups of filters.
- Section verification.
  - OCRC/Checksum verification of assembled sections via hardware DMA engine.

2.12 X-Stream T4 Peripherals

The X-Stream T4 contains supporting peripheral blocks:

- General Purpose I/O Pins - Provide 32 GPIO pins, some of which are overloaded with other functions. (See the "Pin Descriptions" section.)
- ISO 7816 Smart Card interface - One ISO 7816 smart card interface is provided. Smart card interface pins are muxed on GPIO pins.
- 16550 compatible UART - Contains two 16550 compatible UARTs. One is accessible through the PCI interface and the other by the internal processors.
- SPI - Provides one SPI master interface and one SPI slave interface. Both are compatible with the Motorola SPI protocol and the National Semiconductor Microwire/Plus protocol. The master interface is on dedicated pins; the slave interface is muxed on GPIO pins.
- I2C - Provides four I2C master interfaces. Two of the I2C are on dedicated pins; two are muxed on GPIO.
- Copy Protection Cipher Block - Supports the encryption and decryption of DES, TDES and AES128.
- Memory DMA - Includes two general purpose memory-to-memory DMA engines. They support memory fill, linear copies, and rectangular copies.

Section 3 Pin Descriptions

Functional Blocks

The following tables show the various functional blocks and their associated number of pins.

3.1 656 Video Interface Pins

Table 3-1: 656 Video Interfaces

Name	Type	Drive	5 V Tol.	Slew	Schmitt	Pull Up	Pull Down
VID_656_DATA_0	Output	8 mA		Yes	Yes	None	None
VID_656_DATA_1	Output	8 mA		Yes	Yes	None	None
VID_656_DATA_2	Output	8 mA		Yes	Yes	None	None
VID_656_DATA_3	Output	8 mA		Yes	Yes	None	None
VID_656_DATA_4	Output	8 mA		Yes	Yes	None	None
VID_656_DATA_5	Output	8 mA		Yes	Yes	None	None
VID_656_DATA_6	Output	8 mA		Yes	Yes	None	None
VID_656_DATA_7	Output	8 mA		Yes	Yes	None	None
VID_656_CLK	Output	8 mA		Yes	Yes	None	None

3.2 ATA Interface Pins

Table 3-2: ATA Interface Pins

Name	Type	Drive	5 V Tol.	Slew	Schmitt	Pull Up	Pull Down
PDD_01	Bidirectional	12 mA	Yes	Yes	Yes	Fixed	None
PDD_00	Bidirectional	12 mA	Yes	Yes	Yes	Fixed	None
PDD_05	Bidirectional	12 mA	Yes	Yes	Yes	Fixed	None
PDD_04	Bidirectional	12 mA	Yes	Yes	Yes	Fixed	None
PDD_03	Bidirectional	12 mA	Yes	Yes	Yes	Fixed	None
PDD_02	Bidirectional	12 mA	Yes	Yes	Yes	Fixed	None
PDD_09	Bidirectional	12 mA	Yes	Yes	Yes	Fixed	None
PDD_08	Bidirectional	12 mA	Yes	Yes	Yes	Fixed	None
PDD_07	Bidirectional	12 mA	Yes	Yes	Yes	Fixed	None

Table 3-2: ATA Interface Pins (Continued)

Name	Type	Drive	5 V Tol.	Slew	Schmitt	Pull Up	Pull Down
PDD_06	Bidirectional	12 mA	Yes	Yes	Yes	Fixed	None
PDD_13	Bidirectional	12 mA	Yes	Yes	Yes	Fixed	None
PDD_12	Bidirectional	12 mA	Yes	Yes	Yes	Fixed	None
PDD_11	Bidirectional	12 mA	Yes	Yes	Yes	Fixed	None
PDD_10	Bidirectional	12 mA	Yes	Yes	Yes	Fixed	None
PDA_1	Output	12 mA		Yes	Yes	None	None
PDA_0	Output	12 mA		Yes	Yes	None	None
PDD_15	Bidirectional	12 mA	Yes	Yes	Yes	Fixed	None
PDD_14	Bidirectional	12 mA	Yes	Yes	Yes	Fixed	None
PDIOR_N	Output	12 mA		Yes	Yes	None	None
PCS1_N	Output	12 mA		Yes	Yes	None	None
PCS0_N	Output	12 mA		Yes	Yes	None	None
PDA_2	Output	12 mA		Yes	Yes	None	None
PIORDY	Input		Yes			Fixed	None
PDMACK_N	Output	12 mA		Yes	Yes	None	None
PDMARQ	Input		Yes			None	Fixed
PDIOW_N	Output	12 mA		Yes	Yes	None	None
PINTRQ	Input		Yes			Fixed	None

3.3 16-Bit DDR SDRAM Interfaces

Table 3-3: 16-Bit DDR SDRAM Interfaces

Name	Type	Drive	5 V Tol.	Slew	Schmitt	Pull Up	Pull Down
D16_A_04	Output					None	None
D16_A_03	Output					None	None
D16_A_05	Output					None	None
D16_A_02	Output					None	None
D16_A_06	Output					None	None
D16_A_01	Output					None	None
D16_A_07	Output					None	None